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ATOMIC TIME AND FREQUENCY REFERENCE SYSTEM

FINAL REPORT - PART I

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1. INTRODUCTION

This is the final report on Part 1 of Contract No. NAS 9-5425 entered into by NASA-Manned Space Craft Center and Varian Associates of Palo Alto, California on January 13, 1966, for the purpose of developing an atomic time and frequency reference system for manned spacecraft use. The contract is divided into two separately funded parts. Part 1 includes the design study, detailed design, breadboard construction, and breadboard tests of a rubidium atomic time and frequency reference system. Also included in Part 1 is the delivery of two hydrogen masers and the development and construction of additional frequency comparing test equipment for the purpose of measuring the stability of the rubidium frequency standard relative to the hydrogen masers. Part II consists of the construction and testing of two flyable prototype clocks. This document is the final report on Part 1 of the program. The contractual requirements for deliverable items of hardware and software are specified in more detail below.

1.1 HARDWARE REQUIREMENTS

1.1.1 Atomic Time and Frequency Reference System

The contract calls for the delivery of a breadboard atomic time and frequency reference system. This unit, shown in Figure 1, was mounted in a 19" rack cabinet in order to facilitate testing and evaluation at NASA. The unit consists of two major portions, (1) the breadboard of the flyable portion (space clock) which is mounted in the box to the rear of the deck, and (2) a test and calibration unit mounted on

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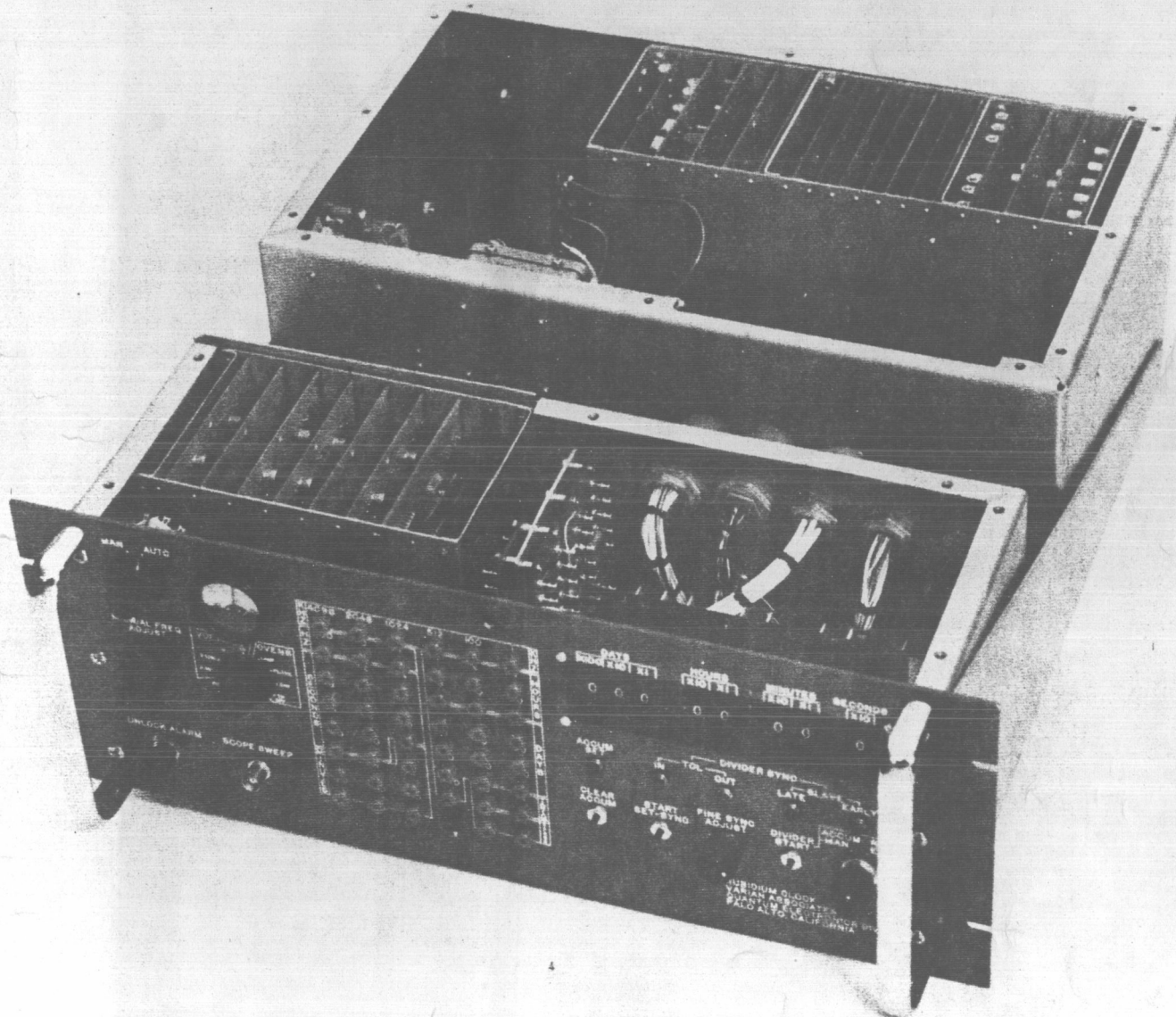


FIGURE 1. ATOMIC TIME AND FREQUENCY REFERENCE SYSTEM

the front of the deck and comprising the front panel of the rack mounted installation. The flyable portion is a completely enclosed frequency standard and clock having four plugs through which power is supplied and standard frequency and time signals are brought out to the outside world. This box is connected to the test and calibration unit by means of three cables. The test and calibration unit enables voltages and wave forms within the frequency standard to be monitored to assure that it is operating properly, and it also contains setting circuits to enable the clock to be set relative to an external master clock to within ± 0.25 microseconds. Connections between the two units can be made or broken without affecting the operation of the frequency standard and clock. Since the test and calibration unit would only be used on the ground prior to actual flight, no re-design of this unit would be necessary in the development of final hardware, and this unit exists in its final design configuration. The purpose of Part 1 of this contract has been to perform an electrical design of the atomic time and frequency reference system which will demonstrate operation over the wide ambient temperature range with low power consumption. The design utilizes physically small and rugged components which lend themselves well to re-design and re-packaging into final flight hardware in Part II of the contract.

1.1.2 Hydrogen Masers and Frequency Comparison Test Equipment

Part 1 of the contract also called for the delivery of two hydrogen masers and the design and construction of frequency comparison test equipment to compare the rubidium standard against the hydrogen masers. A frequency comparator was developed in which a 1 KHz difference

frequency is obtained between outputs of the maser and the rubidium standard at a synthesized frequency of 1,450 KHz. The comparator has two input channels to accept signals from either of the two masers and one input channel to accept the signal from the rubidium standard. The output 1 KHz signal is counted by a period counter, the outputs of which are coupled to a digital to analog converter, a digital printer, and an analog strip chart recorder, all of which were supplied as part of the frequency comparison measuring equipment.

1.2 SOFTWARE REQUIREMENTS

The following items are the software requirements of the contract.

1.2.1 Schematics

Three copies of electrical schematics of the space clock and the test and calibration box were supplied with the units. Detailed mechanical drawings were not supplied since this design is only a bread-board unit and no further units like it are to be manufactured.

1.2.2 Operating Instructions

A set of operating instructions for the clock and test and calibration unit were written and delivered with the equipment.

1.2.3 Reports

Monthly progress reports which described the overall progress, indicated current problem areas, and discussed the work to be performed during the next reporting period were submitted throughout the contract.

The contract also required a final report which documents and summarizes the results of the contractual work, and this report is submitted in response to this requirement.

1.2.4 Procedures for the use of Frequency Comparison Test Equipment

The contract required that procedures be submitted for the use of the specially designed frequency comparison test equipment which was designed and delivered under the contract. An operating manual for the frequency comparator was written which described the use of this equipment in conjunction with the related peripheral frequency measuring equipment. Since this document also discussed the design of the frequency comparator and its performance limitations, no further discussion of this frequency comparator will be given in this final report.

2. DEVELOPMENT OF THE BREADBOARD FREQUENCY STANDARD AND CLOCK

The primary purpose of the contract is to develop an atomic time and frequency reference system which would be capable at some future date of replacing the crystal time and frequency reference systems that are currently being used on manned spacecraft. In order to satisfy this interchangeability requirement, the program philosophy has been to develop an atomic standard on the same time base as the present crystal standards, having output frequencies and time codes which are identical in frequency waveform and level to those obtained from the present crystal standards. The advantage of the atomic time and frequency reference system is of course the attainment of atomic standard stability onboard the spacecraft, an improvement in frequency stability of between 3 and 4 orders of magnitude being obtained over time periods of one week to one year. This improvement is obtained at a modest sacrifice in weight, volume and power due to the greater complexity of the atomic standard in comparison to the crystal standard. Because of this increase in size and power consumption, the atomic standard may not be a direct replacement for the crystal standard in all applications. Major design goals of the development program are to minimize the size, volume and power consumption in order that the interchangeability may be more universal. In addition, the atomic standard must operate over the wide temperature ranges and the severe shock, vibration and acoustic noise environments encountered within the spacecraft, and function reliably over extended periods of unattended operation.

Design goals for the eventual flyable prototypes are:

1. Frequency stability: 2×10^{-11} over a period of one year
2. Size: 300 cubic inches
3. Weight: 10 pounds
4. Power consumption: 15 watts
5. Operating temperature range: -34 to $+71^{\circ}\text{C}$
6. Acceleration: 20 g's
7. Shock: 50 g's
8. Vibration: 15 g's

The steps which have been taken in the development to meet these goals and the compromises which have been necessary to design around certain problem areas are discussed in the following sections.

2.1 ELECTRICAL DESCRIPTION OF EQUIPMENT

A block diagram of the flyable space clock and the associated ground-based test and calibration unit is shown in Figure 2. The space clock generates square wave output signals at a level of 3V p-p into 100 ohms at frequencies of 4.096MHz, 2.048MHz, 1.024MHz, 512KHz, 100KHz, 1KHz, 100Hz, and 1Hz. In addition, 34 parallel output lines supply 5V p-p signals into 1,000 ohms from the one or positive output of each flip-flop in the accumulator from the 0.1 second to the two hundred day flip-flop. Two other lines supply IRIG B and IRIG E serial time codes at the same voltage and impedance levels. The test and calibration unit receives these clock outputs and other signals from the clock and enables performance checks to be carried out on the frequency standard portion, and setting and synchronizing of the clock to be performed.

2.1.1 The Breadboard of the Flyable Space Clock

The clock is divided into four main functional areas for the purpose of discussion:

(1) The Optical Package, which contains the rubidium reference mounted in a triple magnetic shield, and its associated photocell, filter cell and rubidium lamp.

(2) The analog circuits, consisting of the feedback control circuits from the rubidium reference to the crystal oscillator, the crystal oscillator and its oven controller circuits, frequency multipliers and synthesizers to generate the rubidium frequency, the 100KHz synthesizer and the temperature controllers for the optical package.

(3) The digital circuits, consisting of the frequency divider from 16.384MHz to the 200 day flip-flop, time code generators for the IRIG B and IRIG E time codes, and output buffer amplifiers.

(4) The power supply consisting of four regulated output D.C. voltages, one unregulated output D.C. voltage, and A.C. square wave signals for use in the temperature controllers for the optical package.

Photographs of the top and bottom of the space clock are shown in figures 3 and 4.

2.1.1.1 Optical Package

The optical package contains the rubidium vapor reference cell which is filled with a buffer gas. The pressure of the buffer gas is adjusted such that the resonant frequency of the cell is 6,834.688 MHz. This cell is mounted inside a cylindrical microwave cavity tuned to resonance at that frequency in the TE_{011} mode. Light from the

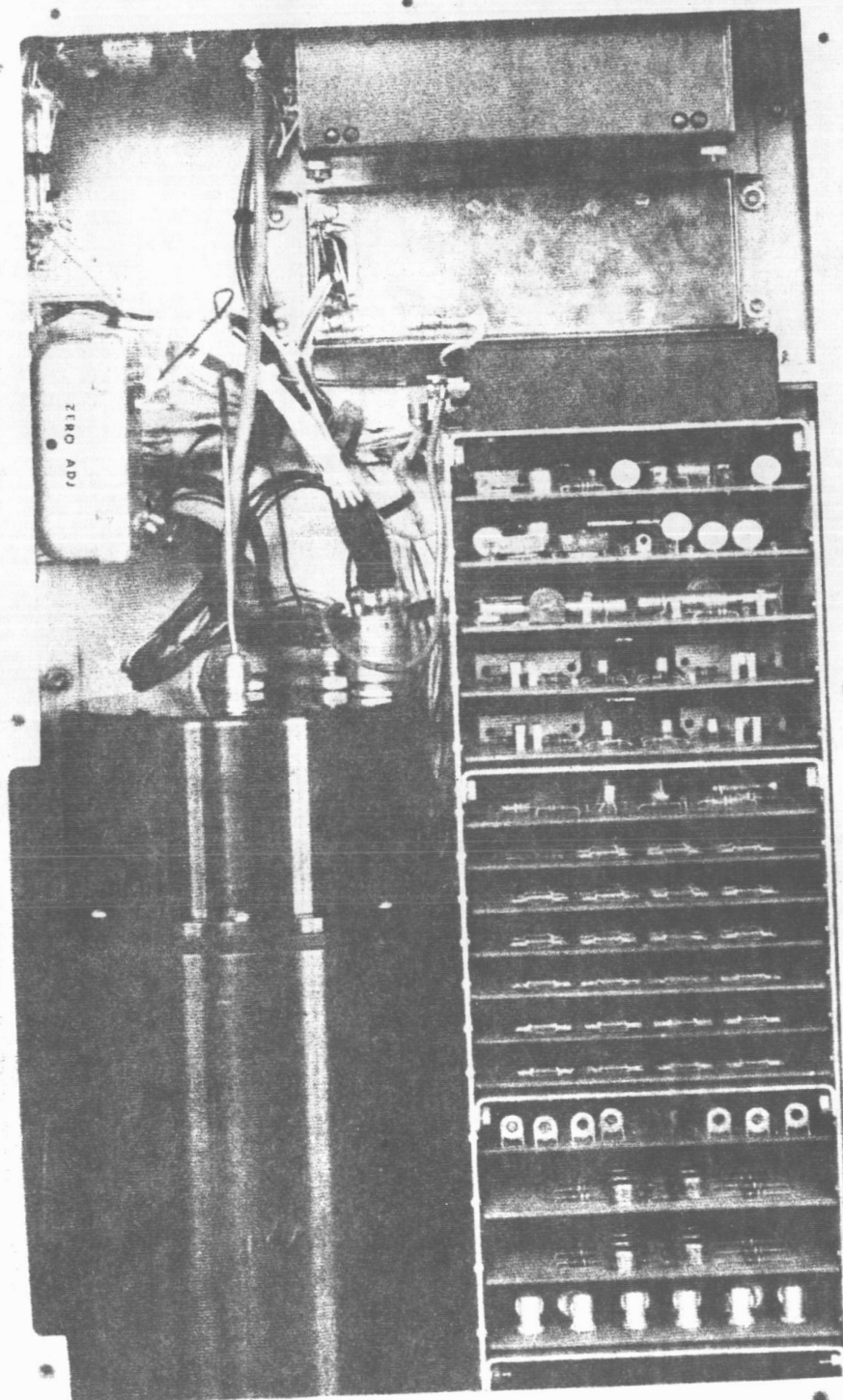


Fig. 3 Space Clock - Top View

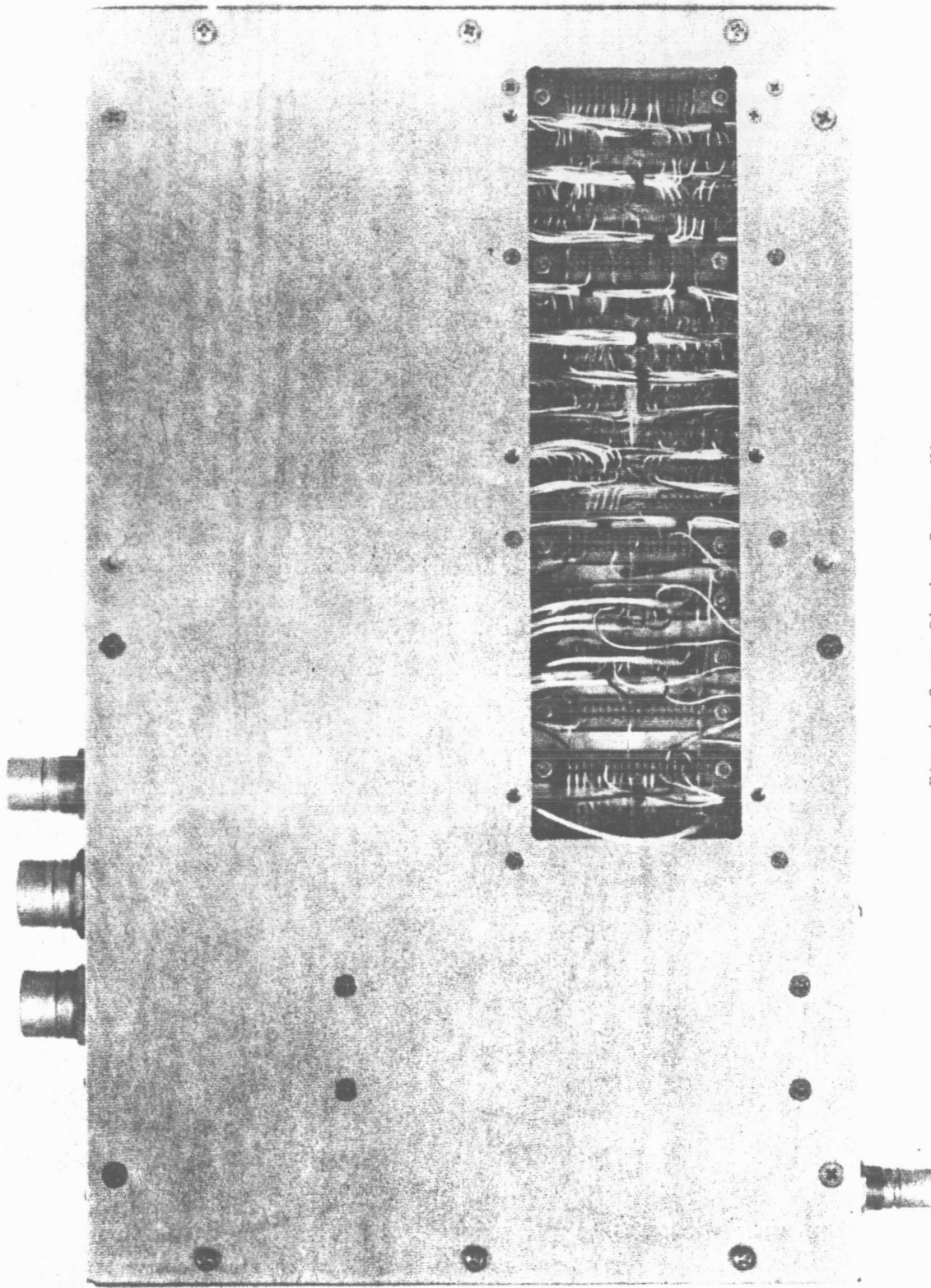


Fig. 4 Space Clock - Bottom View

rubidium lamp optically pumps the gas cell to obtain an increase in the population of atoms in the upper hyperfine energy level, this increase being obtained by inserting a rubidium filter cell between the lamp and the gas cell so as to attenuate the spectral component from the lamp which would normally depump the upper hyperfine level. The total light transmitted through the gas cell is detected by a photocell at the other end of the optical package. The microwave cavity is excited by a signal at 6,834.688 MHz which is the 13,349th harmonic of 512 KHz. The coupling of the A.C. magnetic field in the cavity to the rubidium atoms causes downward transitions between the two hyperfine levels and increases the number of atoms to be repumped to the higher state. Repumping absorbs optical photons and decreases the amount of light incident on the photocell. The microwave signal exciting the cavity is square wave frequency modulated at a rate of approximately 173 Hz. This modulation causes A.C. signals to appear at the photocell having components at the first and second harmonics of the 173 Hz modulation frequency with amplitudes and phases dependent upon the difference between the rubidium reference frequency and the average frequency of the microwave excitation. These signals are used by the feedback control circuits to determine the difference between the excitation and the rubidium reference and to control the crystal oscillator so as to minimize the difference.

The frequency of the rubidium reference changes with temperature variations of different elements in the optical package. The four critical points which are controlled by temperature controllers are:

- (1) the body of the rubidium reference cell as determined by the temperature

of the microwave cavity, (2) the tip-off of this reference cell, (3) the rubidium filter cell, and (4) rubidium lamp.

The frequency of the rubidium reference is also a function of the magnetic field experienced by the rubidium atoms. The hyperfine transition which is used for the reference has no first order magnetic field dependence, however, there is a second order dependence which causes the frequency to be:

$$f = 6,834,682,614 + 574H^2 \text{ Hz}$$

for zero buffer gas pressure, where H is the magnetic field in gauss.

The reference frequency used in the space clock requires that the rubidium reference be offset by 5,386 Hz or 7.9×10^{-7} from the zero field, zero pressure frequency. The cell is filled low in frequency by $3 \pm 2 \times 10^{-9}$ by controlling the buffer gas pressure, and then is tuned up to the proper frequency by setting the magnetic field with field bias control circuits. The reference is mounted inside a triple magnetic shield to reduce ambient magnetic fields to a negligibly small level, and the field bias circuits create an internal field of the proper magnitude. This field is permanently set for a given gas cell. A fine tuning adjustment is provided for tuning the frequency over a total range of $\pm 5 \times 10^{-11}$ from the factory pre-set frequency.

2.1.1.2 Analog Circuits

The analog circuits consist of all of the elements of the frequency locked loop with the exception of the optical package. The AGC stabilized crystal oscillator runs at a frequency of 16.384 MHz and has two separately buffered outputs. The first of these outputs drives a digital divider chain consisting of integrated circuit digital dividers. The first division by four is performed by a Sylvania

50 MHz dual flip-flop. The resulting square wave output at 4.096 MHz is fed to a 5th harmonic filter amplifier which selects the component at 20.480 MHz. This signal is squarewave frequency modulated at 173 Hz and fed to the high frequency multiplier. The high frequency multiplier performs an initial multiplication by 9 to generate 184.32 MHz, followed by a multiplication by 37 to generate 6,819.84 MHz. This signal is fed to a mixer in which the final rubidium frequency is generated. The other input to the mixer is obtained by taking the 512 KHz squarewave from the digital divider chain, selecting the 3rd harmonic of this signal, at 1.536 MHz, in a filter amplifier, and subtracting this frequency from the 16.384 MHz signal obtained from the second output of the crystal oscillator. The resulting signal at 14.848 MHz is added to the 6,819.84 MHz signal in the high frequency multiplier to generate the rubidium excitation frequency at 6,834.688 MHz. This signal is fed into the microwave cavity on a 50 ohm coax and is coupled to the cavity by means of a loop whose dimensions are chosen so as to match the 50 ohm line at the cavity resonant frequency.

The interaction between the frequency modulated microwave signal and the rubidium atoms causes a variation in the current produced by the large-area photocell. The output from the photocell is coupled to an integrated circuit preamplifier which has a large amount of DC feedback in order to maintain the voltage across the photocell within a few millivolts of zero in order to prevent the generation of excess noise in the photocell. A small amount of AC feedback is used in the preamp in order to obtain reasonable gain while also presenting low AC amplifier input impedance to the photocell at 173 and 346 Mz.

The DC output from the preamp is used to detect whether the lamp is on and running at the proper output level. At initial turn-on the lamp output is low until the lamp comes up to its proper operating temperature. During this time the DC level from the preamp actuates the lamp starting switch which applies the 24-37V DC input voltage to the lamp oscillator. When the lamp comes up to temperature and the proper light intensity is obtained, the DC level from the preamp rises, turning off the lamp starting switch and applying 12 volts DC to the lamp for continuous operation. This has the dual advantages of allowing the lamp to run from a regulated supply and to consume less power.

The AC outputs from the preamp are coupled to a MOS FET synchronous switch running at the second harmonic frequency, 346 Hz. This synchronous switch converts the second harmonic signal to DC and produces a chopped version of the first harmonic signal, having spectral components at the first harmonic frequency and its odd harmonics. At the output of the amplifier following this synchronous switch, low pass and high pass filters allows separation of the second harmonic information from the first harmonic signal. The second harmonic information, now DC, is used to drive a MOS FET alarm gate which turns on the scan oscillator when the second harmonic declines below a preset threshold level. The scan oscillator sweeps the crystal oscillator frequency in order to search for the rubidium resonance and re-establish lock. The output of the alarm gate is also fed through external cabling to the test and calibration unit to turn on a holding unlock alarm light which indicates that a momentary unlock alarm condition has occurred.

The first harmonic signal information obtained at the output of the high pass filter following the second stage amplifier is fed to a second MOS FET synchronous switch running at 173 Hz which converts the chopped harmonic signal to a DC voltage. This signal is amplified by a third integrated circuit operational amplifier running as an integrator, and it provides the correction voltage to the crystal oscillator for locking the frequency locked loop. A roll-off network between the integrating amplifier and the crystal oscillator shapes the loop gain function in order to obtain high DC gain while guaranteeing that the frequency locked loop will be stable at its maximum obtained band width of approximately 75 Hz.

The signals for frequency modulation and synchronous detection are produced by a uni-junction oscillator running at 692 Hz, followed by two flip-flop dividers which produce 346 and 173 Hz squarewaves. An integrated circuit flip-flop follows the second divider and is used to generate a phase shifted squarewave at 173 Hz for frequency modulation. An amplitude adjustment on the output of the phase shifter allows the correct modulation level to be set. The phase shifter allows the modulation phase to be advanced in order to compensate for the phase delay produced in the optical package.

The temperature controller for the crystal oscillator is built inside the oscillator housing and consists of a DC bridge driving the proportional control oven. Power for the heater is obtained directly from the 24-37V input line.

The four temperature controllers for the optical package consist of AC thermistor bridges which are driven by squarewaves of approximately 3.1 KHz obtained from the DC to DC converter oscillator

in the power supply. Each controller consists of an operational amplifier to amplify the bridge voltage, a synchronous detector, and a DC amplifier which controls the duty cycle of a 3.1 KHz heater pulse. All four heaters are duty cycle modulated in order to obtain maximum efficiency and reduce power consumption. Of the five heaters in the frequency standard four use the raw DC input voltage. The tip-off heater is run from a 6 volt regulated supply because the low mass to be heated and the small amount of power required.

The final portion of the analog circuitry is the 100 KHz synthesizer, which take squarewave inputs from the digital divider at frequencies of 256 KHz, 128 KHz, and 16 KHz. The synthesizer adds 16 KHz to 128 KHz generating 144 KHz, and then adds 256 KHz to obtain 400 KHz. This frequency is divided by 4 in integrated circuits flip-flops to generate the 100 KHz squarewave output.

2.1.1.3 Digital Circuits

The digital circuits consist of the frequency divider which divides 16.384 MHz down to 1 Hz, the accumulator which performs additional division, accumulating seconds, minutes, hours, and days to a maximum count of 400 days, and the digital circuits which generate time code in the IRIG B and IRIG E formats. Also included in the digital circuits are nine output amplifiers for frequencies from 4.096 MHz down to 1 Hz, 34 amplifiers providing parallel time code outputs from 0.1 cycles per second to 200 days and two output amplifiers supplying IRIG B and IRIG E time codes.

The first division by 4 in the divider chain is performed by a Sylvania dual 50 MHz flip flop. The next division by 8 from 4.096 MHz to 512 KHz is performed by medium speed Fairchild diode transistor micrologic flip flops. The remainder of the digital circuits which include the rest of the divider, the accumulator, and the IRIG time code generators use low power Fairchild diode-transistor micrologic integrated circuits.

The output amplifiers for all 45 output channels are PNP transistors which are turned on in order to supply current to the load in the high voltage, or one state, and are turned off for the zero state. The 9 output amplifiers, from 4.096 MHz to 1 Hz, which supply three volt p-p signals into 100 ohm loads, have 56 ohm emitter resistors in order to divide the 5 volt supply down to 3 volts across the load. The other 36 output amplifier which supply

5 volts p-p into 1,000 ohms, have no emitter resistance and switch the 5 volts directly from the power supply to the load. This design approach was taken in order to minimize the total power consumption, however, it does mean that the latter amplifiers are not short circuit protected.

2.1.1.4 Power Supply

The power supply consists of an input coarse voltage regulator of the switching type which converts the input 24 to 37 volts to a 22 volt DC output. The DC to DC converter oscillator runs from this 22 volt supply at a frequency of approximately 3.1 KHz. Multiple taps on the transformer in the oscillator supply square wave signals to regulated and unregulated output lines. Four regulated DC output voltages are provided with dissipated regulators in each output. The regulated voltages are 20 volts, 12 volts, and two separate outputs at 5 volts. The 20 volt supply is used to run all of the analog circuits of the clock. The 12 volt supply is used exclusively for continuous operation of the rubidium lamp oscillator. One of the five volt outputs, which has a 1 watt capability, is used for all of the five volt requirements within the frequency locked loop. These requirements are: the bias for the lamp oscillator, the digital dividers from 16.384 MHz down to 512 KHz, and the 4 output amplifiers from 4.096 MHz through 512 KHz. The other 5 volt regulated output, which has a 3 watt capability, is used for all of the lower frequency digital circuits and output amplifiers. Separate 5 volt lines are used in order to prevent the lower

frequency signals from leaking into the multiplier and synthesizer of the rubidium frequency in order to prevent spurious sidebands in the microwave spectrum.

Another winding on the DC to DC converter transformer is a center tapped winding having 13 volts p-p on each side with respect to the center tap. These signals are rectified to provide a coarsely regulated 6 volt output which supplies power to the tip-off heater. The 13 volt p-p signals are used by the four optical package oven controllers for the purpose of synchronous detection and generation of the pulse-width-modulated duty cycle. Another winding on the DC to DC converter transformer supplies square wave signals at 0.7 and 3.5 volts p-p for use in the temperature bridges of the 4 optical package temperature controllers.

Power for all of the heaters with the exception of the tipoff heater is taken directly from the input line ahead of the power supply in order to obtain best efficiency and reduce power consumption. The power supply and these heater circuits are all reverse voltage protected so that no damage will occur to the unit by inadvertent polarity reversal of the input. In final flight hardware an RFI filter will be used at the power input plug, but this is not incorporated in the breadboard unit. The power supply, however, has been designed in order to minimize conductive interference.

2.1.2 Test and Calibration Unit

The test and calibration unit shown in Figures 5 and 6 has been designed as a piece of ground-based test equipment which enables the frequency standard to be checked out prior to flight and contains the digital circuits for setting the clock to within a microsecond of an external master clock. This unit can be connected to the clock for all final calibration and testing and can be disconnected without disrupting the operation of the clock.

The test and calibration unit is divided into three major circuit areas as follows:

- (1) Monitor and control circuits, consisting of a multimeter for monitoring d.c. voltages, oven control points, and signal levels in the frequency standard; manual frequency control circuits; and an unlock alarm indicator.
- (2) Digital clock setting circuits, for the purpose of setting the time accumulator and synchronizing the divider in the space clock.
- (3) A power module, for generating a regulated 5v d.c. for operation of the digital clock setting circuits.

2.1.2.1 Monitor and Control Circuits

The monitor and control circuits enable the operator to check the operation of the frequency standard portion of the space clock. A multiple-

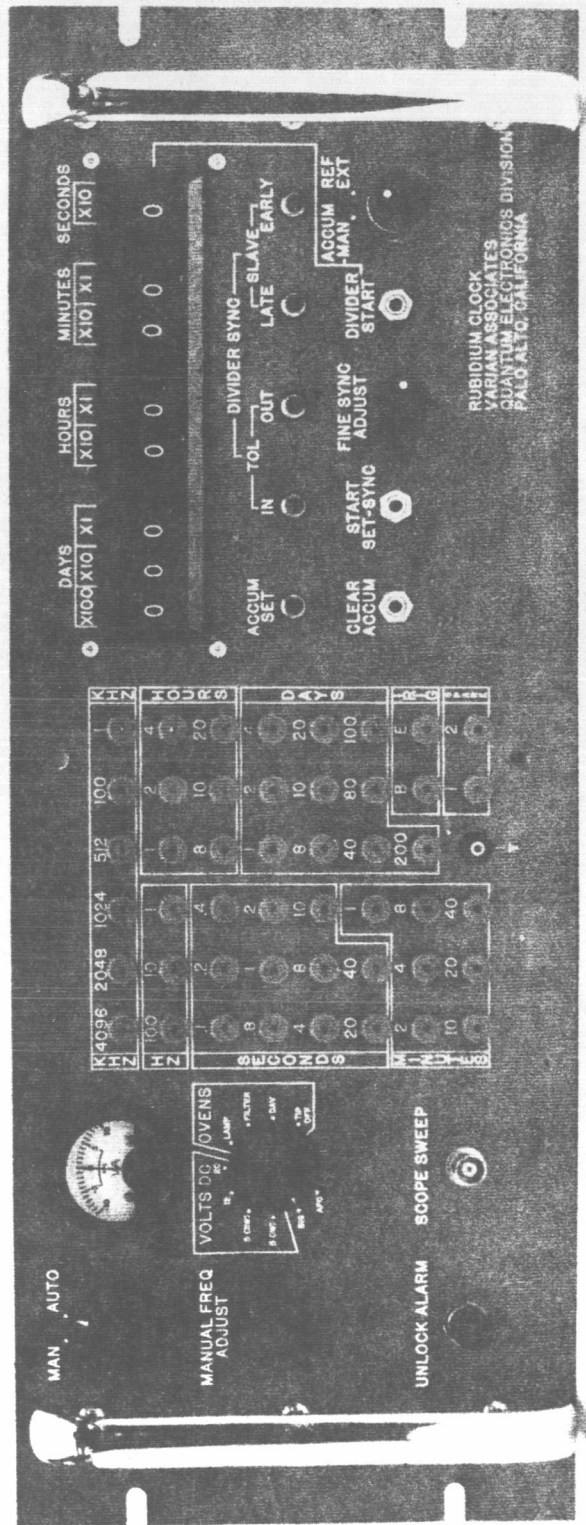


Fig. 5 Test and Calibration Unit - Front View

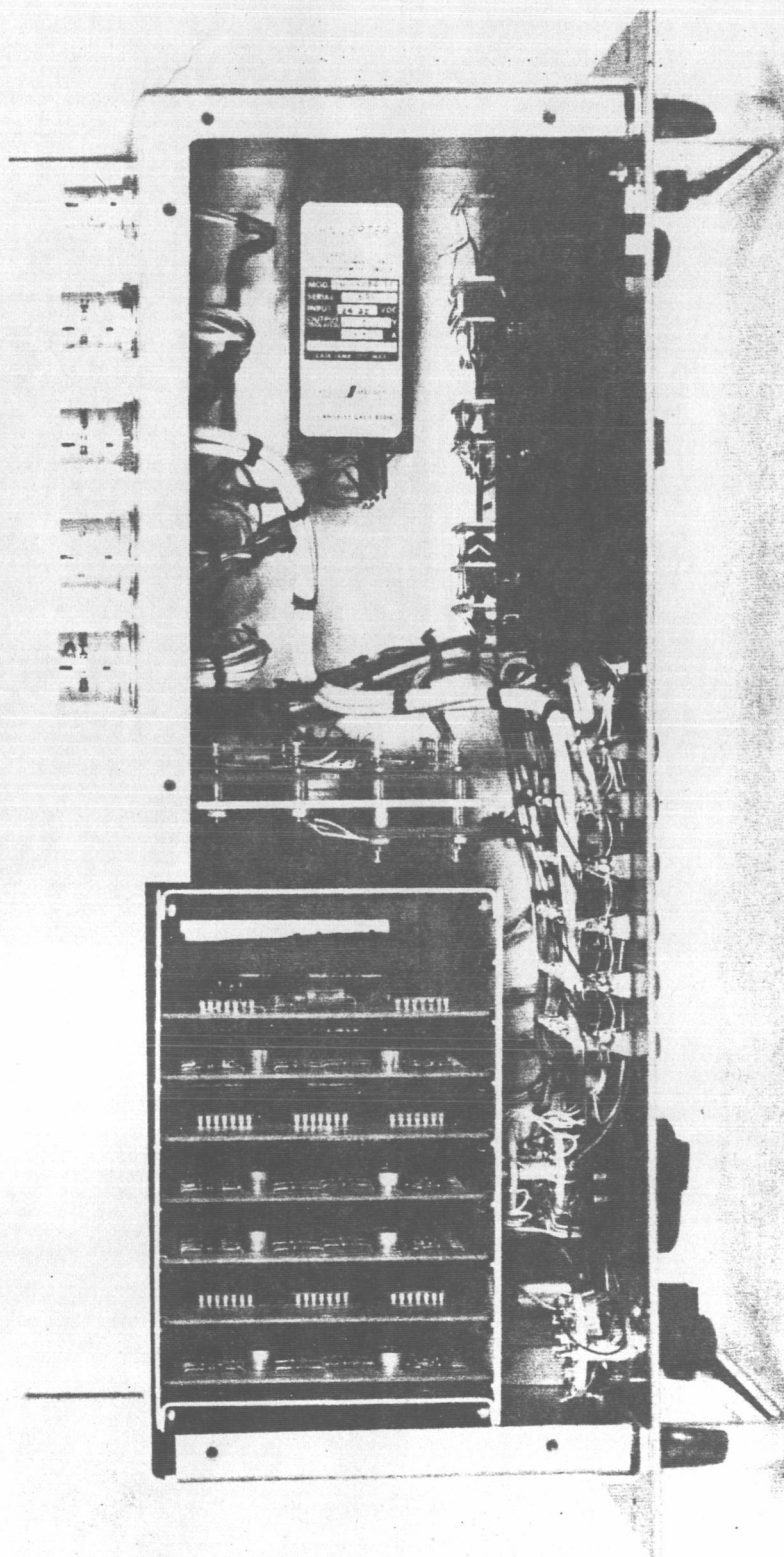


Figure 6. Test and Calibration Unit - Top View

position switch and meter allows monitoring of the second harmonic signal level at the output of the second servo amplifier, the automatic frequency control signal applied to the crystal oscillator at the output of the third amplifier, the four regulated DC power supply voltages, and the duty cycle of the four ovens in the optical package.

A switch enables the clock to be set to either the automatic or manual frequency control modes. In the auto mode the servo loop seeks a frequency lock utilizing the internal scan oscillator. The space clock operates in this auto mode when the cable to the test and calibration unit is disconnected and is only prevented from operating in the auto mode when the mode switch is in the manual frequency position. In the manual position the servo loop is opened, the scan oscillator is disconnected, and the manual frequency adjust potentiometer on the front of the test and calibration unit allows a variable DC AFC voltage to be applied to the crystal oscillator for tuning it over a range of $\pm 2-3 \times 10^{-6}$ with respect to its normal setting. This manual mode is useful for observing the resonance line in the optical package, or for obtaining large unlocked frequency offsets. The AFC meter reading is used for setting the control signal to zero by adjusting the crystal trim potentiometer on the space clock chassis prior to flight.

A BNC jack on the front of the test and calibration unit brings

out a sawtooth voltage at the modulation frequency of 173 Hz which is used either as a means of monitoring the modulation frequency to determine if the modulation oscillator is functioning properly, or as a voltage to provide horizontal sweep for an oscilloscope when monitoring the signal levels at the output of the preamplifier in the servo loop during initial setting and/or maintenance of the clock.

The monitor and control circuits also include an unlock alarm light which is turned on by an SCR locking switch if an unlock alarm occurs in the frequency locked loop. This light remains on until the light is pushed, in which case the turn off switch will extinguish the light if an unlock alarm condition does not still exist in the servo loop.

All of the lines for the monitor and control circuits are brought from the space clock to the test and calibration unit on a single multi-conductor cable.

2.1.2.2 Digital Clock Setting Circuits

The clock setting circuits consists of a time comparator which compares the 30 accumulator output lines from seconds 1 through days 200 with 30 similar data lines from a master clock. A button is provided which enables the operator to initiate calibration of this slave clock by setting the accumulator and synchronizing the divider in the space clock. If the

space clock accumulator does not agree with the master clock, the 100 KHz signal from the space clock is used to run up the accumulator at the 1 cps input, thus running up the accumulator a factor of 10^5 faster than it normally operates. When the two clocks agree, the 100 KHz signal is turned off and the falling edge of the 1 Hz signal in the divider is then synchronized to the same falling edge of the 1 Hz signal from the master clock. Setting of the space clock is then complete. Lights on the front panel of the test and calibration unit indicate whether the space clock is set, whether the setting has fallen within the \pm microsecond setting tolerance, and whether the space clock is late or early with respect to the master clock. A fine sync adjust potentiometer allows a continuous adjustment of approximately 1 microsecond to be made in the relative setting between the two clocks for finer synchronization.

In the event that no master clock is available, a set of manual switches has been provided which enables days, hours, minutes, and tens of seconds to be manually inserted into the space clock accumulator. In this mode of operation the divider is started by means of depressing a push button and of course no synchronization to an external reference occurs.

After resetting of the space clock, the master clock inputs and the cable carrying the digital signals between the space clock and the test and calibration unit can be left connected or disconnected as desired. If left

connected, the late-early circuits continue to tell whether the space clock is ahead or behind the master clock in time calibration and the tolerance lights indicate whether a time error larger than one microsecond has accumulated.

Also on the front of the test and calibration unit are 45 signal level test points for monitoring all the outputs of the space clock. All of these lines are loaded by their proper impedances within the test and calibration unit, the nine outputs from 4.096 Mc to 1 cps being loaded with 100 ohms, and the other 34 outputs lines being loading with 1000 ohms.

2.1.2.3 Power Module

A power module within the test and calibration unit takes 24 to 32 volts DC as an input, and, by means of a DC to DC converter and voltage regulator, produces 5 volts DC for operation of all the digital clock setting circuits.

The monitor and control circuits within the test and calibration unit derive all of their power from the space clock itself and no power input to the test and calibration unit is required if the digital clock setting circuits are not to be used. However, care must be taken to disconnect the digital circuit cable connecting the space clock to the test and calibration unit prior to removing power, since failure to do so, will ground the reset line and stop the clock.

2.2 Major Design Problem Areas

The development of the atomic time and frequency reference system has presented a number of difficult and challenging design problem areas which have required new technical approaches and, in some cases, trade-offs between desired design goals. The most difficult design problem has been that of obtaining satisfactory operation of the space clock under the combinations of severe environmental conditions. In addition, some new design approaches have been necessary in order to separate the monitor and control functions from the flyable space clock and place them in a ground based unit.

2.2.1 Space Clock

The major design problem areas for the flyable space clock unit are:

1. Thermal design, which includes the design for high temperature operation (71°C), the design for wide temperature range, the design for minimum power consumption, and the design for the best compromise between the conflicting requirements of mechanical rigidity and minimum power consumption while maintaining adequate temperature control.

2. Mechanical design, which includes design for the high shock and vibration environment, design for minimum size consistent with minimizing power consumption and maximizing rigidity, and sealing the unit for RFI protection and for immunity to environmental pressure and gas composition changes.

3. The design for long term unattended operation. The way in

which these difficult design problem areas manifest themselves in the various parts of the space clock is discussed in the following sections.

2.2.1.1 Optical Package

The development of an optical package which would operate at elevated temperatures had been foreseen to be, and in fact, proved to be the most difficult problem in the breadboard development. During the course of the program, two different approaches to the thermal design of the optical package were tried, which are shown in block diagram form in Figure 7. In both of these designs, the lamp was located outside of the triply-magnetic-shielded region, with temperature controls at $+116^{\circ}\text{C}$, and its light was brought through the shield cans by means of a light pipe.

The first thermal design, Figure 7a, was a minimum power solution to the temperature control problem. In this design the tip-off of the reference cell was heat-sunk directly to the hermetically sealed aluminum housing surrounding the triple magnetic shield and was controlled by means of a heater mounted on the tip-off itself. The microwave cavity served as the oven for the body of the reference cell and also functioned as an outer oven for the filter cell which was mounted inside the cavity structure and incorporated its own oven. The photocell was in good thermal contact with the innermost magnetic shield. The problems with this design were that both the cavity and the tip-off heaters had to control against the total environmental temperature range, which increased the

tendency of the temperature controllers to oscillate because of the large duty cycle variation encountered over the combination of ambient-temperature and input power-supply-voltage ranges. In addition, the degree of thermal control was not as tight as desired and the configuration of the ovens introduced substantial thermal gradients within the optical-microwave structure. In this design, the filter cell was operated at 89°C, the body of the reference cell at 84°C, and the tip-off of the reference cell at 76°C. The temperature of the photocell varied from 56 to 75°C over an ambient temperature range of -34 to +71°C. It was possible to obtain satisfactory signal levels and maintain frequency lock over this entire ambient temperature range, however, the internal thermal gradients and the lack of desired temperature control caused a frequency change of approximately 1.6×10^{-9} over the temperature range, with a slope of $-2 \times 10^{-11}/^{\circ}\text{C}$ at room temperature. In addition, the temperature variation of the photocell caused variation of the output signal level which was a minor problem. In this design, the smallest mass heater, namely that of the tip-off, was powered from a regulated 6V supply while the remainder of the heaters were run from the unregulated 24 to 37V input. Variation of input voltage also caused a frequency change of approximately 2.6×10^{-10} over the 24 to 37V range in measurements made at room temperature. It is believed that this variation was caused by variations in the filter cell temperature since this is the most thermally critical element in the entire standard, its temperature sensitivity being 5×10^{-10} per $^{\circ}\text{C}$ at the elevated operating temperature.

Since the frequency variation with temperature was so large that it precluded making meaningful long term stability measurements unless the clock were operated at extremely constant ambient temperature, a major modification in the heater design was carried out. In this design, Figure 7b, the innermost magnetic shield is operated as an outer oven with the tip-off of the reference cell in good thermal contact with the shield. The cavity is operated as an inner oven which controls the body of the reference cell and serves as an outer oven for the filter cell. The filter cell is therefore operating in a triple oven configuration. In this design the photocell is heat-sunk to the cavity and operated at a higher but more constant temperature. This elevated temperature reduces the efficiency of the photocell and required that the operating temperatures be reduced in order to obtain satisfactory signal levels. Internal temperatures are 85°C for the filter cell, 80°C for the body of the reference cell, the microwave cavity, and the photocell, and 73°C for the outer oven and tip-off of the reference cell. This configuration has resulted in a significant reduction in the internal gradients because of the presence of the outer oven, and has improved the control of the photocell and reference cell temperatures because of the presence of the outer oven. The slope of the frequency change at room temperature was improved by greater than a factor of 3, being $-0.6 \times 10^{-11}/^{\circ}\text{C}$ in the new design. This design required that the maximum ambient operating temperature be reduced because of the reduction required in internal temperatures. The power consumption of the entire clock was increased from 21 to 24W at room temperature due primarily to the significantly increased area of the outer oven and its heat

leakage to the ambient environment. In this design, the filter cell is the lowest mass oven and is run from a regulated 6V supply, while the other ovens obtain their power from the unregulated 24 to 37V input. This design improved the frequency vs. input voltage characteristics by a factor of 5 to a total variation of 5.5×10^{-11} over the 24 to 37V input range.

Thermal losses to the environment were largely dictated by the size and the degree of mechanical ruggedness built into the optical package. The unit was designed to operate in the specified shock and vibration environments, and thus has the difficult mechanical-thermal compromises incorporated. The unit was designed as a hermetically sealed case in order to avoid changes in the thermal characteristics caused by wide ambient pressure variations, and it incorporates a double-walled gas cell to minimize frequency changes due to pressure variations caused by the wide ambient temperature range. After the commitment to this particular mechanical design had been made, it was discovered that the lamp could be operated on 0.5W of d.c. input power, which was much lower than had previously been thought possible. It is now believed that because of this lower operating power the lamp could be moved inside one or more of the shields and temperature controlled at that point, giving a smaller, lower-power-consumption unit. This is one of the questions to be resolved in the second phase of the program.

The significance of the work carried out on the optical package is that a unit has been built which, to the best of our knowledge,

operates at higher ambient and internal temperatures than any rubidium standard heretofore constructed, operates over a wider temperature range and with less power consumption than previous units, and incorporates rugged mechanical design features for the shock and vibration environment.

2.2.1.2 Analog Circuits

The frequency of the crystal oscillator was selected as 16.384 MHz, the fourth harmonic of the highest output frequency of 4.096 MHz, in order to achieve the best compromise between (1) a small mass crystal to best withstand shock and vibration, (2) a crystal with low aging rate, and (3) an oscillator with good short term stability. The crystal oscillator was purchased from Frequency Electronics with specifications on long term frequency drift less than $\pm 1 \times 10^{-6}$ in two years, frequency change with temperature less than $\pm 3 \times 10^{-7}$ over the maximum operating temperature range, and short term stability of 3×10^{-11} rms for one second averaging times. In view of these specifications, the dynamic range of the AFC loop was designed to have a maximum frequency correcting range of $\pm 2.5 \times 10^{-6}$ in order to provide sufficient correction range for two years of drift in the crystal oscillator. In addition, a crystal trim control was added to the crystal oscillator which also has the range of $\pm 2.5 \times 10^{-6}$ in order to set the servo loop to the center of its dynamic range at the time of initial calibration. The d.c. gain of the servo loop is approximately $3 \times 10^{+6}$ thus causing the frequency change of the crystal oscillator with temperature to contribute approximately $\pm 1 \times 10^{-13}$ to the output frequency of the standard

over the environmental temperature range. The modulation frequency was set as high as possible, 173 Hz, in order to obtain minimum response time and maximum bandwidth in the frequency lock servo, to obtain the most correction of crystal oscillator noise, and to obtain some degree of correction under vibration conditions. The resulting bandwidth of the servo is approximately 75 Hz. The crystal oscillator meets the frequency vs. temperature specifications, but is significantly worse than the 3×10^{-11} short term specifications, its short term stability being on the order of 12×10^{-11} . Although the crystal oscillator is not the primary contributor to the short term stability of the overall standard for one second averaging times, its contribution is far larger than the short term specification of 5×10^{-12} .

A new design for separation of the first and second harmonics of the modulation frequency in the feedback control circuits was used. This design uses dual synchronous detection at both 2nd and 1st harmonics and requires a modulation oscillator running at the 4th harmonic of the modulation frequency. This design approach in combination with square wave frequency modulation has eliminated the need for large, heavy filters in both the modulating and de-modulating circuits, thus lending these circuits to high density and low volume packaging in the second phase program.

In the synthesis of the frequency which excites the rubidium transition, the design approach was taken to perform all multiplication and synthesis external to the optical package and couple the output of

this synthesizer to the microwave cavity by means of a 50 ohm coaxial line which is matched to the cavity with low standing wave ratio. This design approach runs the risk that the power which excites the rubidium transition may not be constant over the environmental temperature range because the multiplier and synthesizer are not temperature controlled. Satisfactory power-temperature characteristics have been obtained in units of almost identical design built for the commercial R-20's but the units built for the space clock have had power variations larger than desired. With the first thermal design of the optical package, the signal level from the photocell was large enough so that lock could be maintained over the -34 to $+71^{\circ}\text{C}$ temperature range, however the signal level variation with temperature was much larger than desired. With the second thermal design at the optical package, signal levels were lower due to the higher photocell temperature and the reduction in multiplier output power at high temperatures caused the signal level to fall to the point where lock was lost at some temperature between 45 and 61°C . The space clock multipliers should be satisfactory if they can be adjusted to be comparable to those built for the R-20. The reason for the difference is to be investigated in phase II.

The heater controllers for the optical package were designed as duty cycle modulated switching controllers running at approximately 3.1 KHz . Duty cycle controllers are a minimum power consumption approach, but because of the large currents and voltages switched in the heater circuits, spurious signals at 3.1 KHz are found in many parts of the

circuitry. No major attempt has been made to eliminate or reduce these spurious signals since the coupling is dependent upon circuit layout. Since the layout of the engineering model will be significantly different from that of the breadboard, it did not appear worth while to attempt to solve this problem in the breadboard circuitry. The same heater design approach has been taken in the commercial rubidium frequency standards, and it has been found that the spurious signals can be reduced to the point where they produce side bands on the output frequencies of the standard which are greater than 100 db below the output carriers. In the breadboard spaceclock these signals are greater than 80 db below the output signal without any attempt to control them. Significant improvements in this area should be made in the engineering model.

2.2.1.3 Digital Circuits

The primary problem in the digital circuit area was that of selecting a low power integrated circuit logic family having high reliability. A new Fairchild low power diode transistor micrologic family was selected and has proved to be very satisfactory. This is currently the lowest power logic family commercially available. Its speed is high enough to be used for all logic functions below 512 KHz. in the clock. Ordinary diode transistor micrologic elements are used for frequencies above 512 KHz.

Minimum power consumption output buffer amplifiers were designed by using saturating pnp switching transistors which are turned on between the 5v supply and the output load. For those outputs requiring 3v p-p, emitter resistors protect the pnp switches from burn out in the event of short circuits. For those outputs requiring 5v p-p, there are no emitter resistors and the transistor switches are not short-circuit protected. This feature is to be changed according to the revised specifications for the engineering models which require all outputs to be short circuit protected. Slightly more power is required to insure short circuit protection, since a 6v supply will be needed to supply the same current now being provided for the 5v supply.

2.2.1.4 Power Supply

The power supply of the space clock was designed on a sub-contract to Gulton Industries. It uses an input coarse voltage regulator of the switching type followed by a dc to dc converter and dissipative regulators for the four regulated output lines. Overall efficiency of the supply is approximately 64% which is reasonable for a supply of this type operating over the wide range of input voltages required.

One of the problems in the temperature control circuits is to obtain well balanced signals for driving the thermistor bridges. AC bridges are used in order that very stable reference signals can be obtained and stable gain of the low level bridge output signals can be obtained. Taps on the dc to dc converter transformer in the power supply are used to supply the bridge voltages since inductor division of this type provides excellent bridge ratio stability over wide ranges of environmental and operating conditions.

2.2.2. Test and Calibration Unit

There were two major design problem areas in the test and calibration unit; 1) those associated with separating the monitor and control functions and mounting them in a separate chassis, and 2) providing clock setting circuits which would calibrate the clock to a time accuracy commensurate with its inherent stability and accuracy.

The design approach taken for the monitor and control circuits was to build the clock so that it operated in the automatic scan and lock-up mode with no external cable connections, but so that the servo loop can be broken and the crystal manually tuned by connecting a multi-conductor cable to the test and calibration unit, then switching to manual operation. This concept required a new type of design for the feedback control circuits and required that certain signal points within the feedback control circuits be brought out through the multi-conductor cable to the test and calibration unit. It has been found that coupling of modulation and demodulation signals between different lines in the cable connecting the two units causes frequency offsets to be created within the feedback control circuits which can cause frequency steps when the cable is connected or disconnected. In the breadboard unit using a cable 4-1/2 feet long, a frequency step of 2.5×10^{-10} occurs when the cable is disconnected at the space clock end, whereas disconnection at the other end causes a frequency step of 8×10^{-12} . Again this is a problem where layout and shielding is significant and no major attempt has been made to solve this problem in the breadboard unit. In the second phase of the program additional consideration will be given to this problem and the solution will most likely be the use of shielded cables or the elimination of some of the monitor and control functions in the test and calibration unit. In either case an upper limit will most likely have to be placed on the length of the cable separating the two units in

order to prevent coupling interactions.

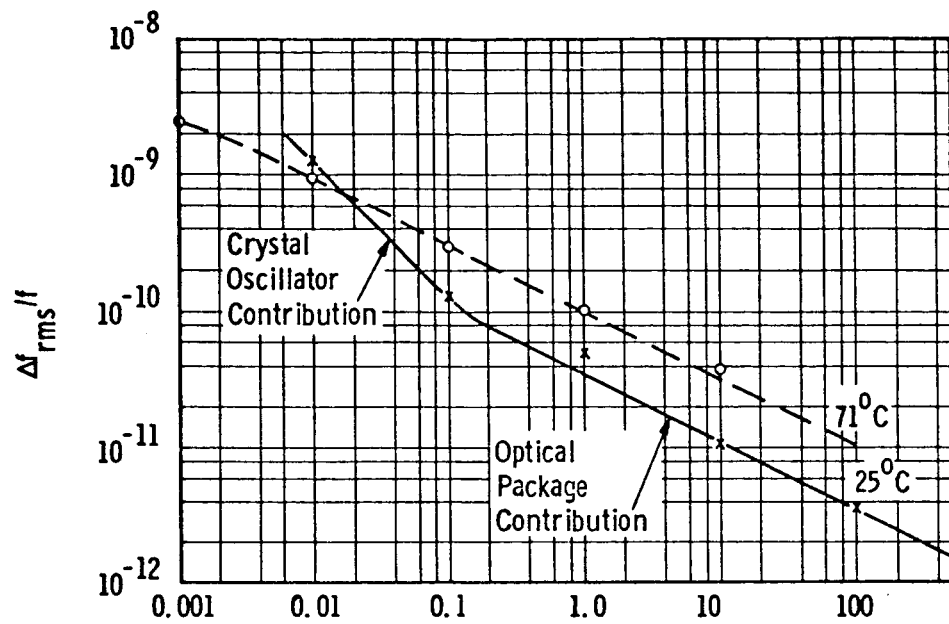
It was decided to design the clock setting circuits so that the space clock could be time calibrated with respect to a master clock within ± 1 microsecond. Time calibration to better than 1 microsecond requires that the point in space at which the time calibration is to be carried out is well defined, since 1 microsecond corresponds to a free space propagation distance of approximately 1000 feet. The test and calibration unit is used as the point in space where time coincidence is monitored. The time coincidence circuits in the test and calibration unit compare falling edges of the 1 Hz signals received from the space clock and the master clock at the ends of their respective connecting cables, and the time calibration of the space clock is performed so as to bring these two signals into time coincidence within ± 1 microsecond within the test and calibration unit chassis. Delay times in the space clock divider chain are eliminated by setting the divider approximately 3 microseconds ahead, and by providing a continuous fine tuning adjustment having a range of ± 0.5 microseconds with respect to the 3 microsecond time advance. This approach to the time calibration should be sufficient for all situations in which the connecting cables do not exceed a few hundred feet.

2.3 Results achieved in the breadboard unit

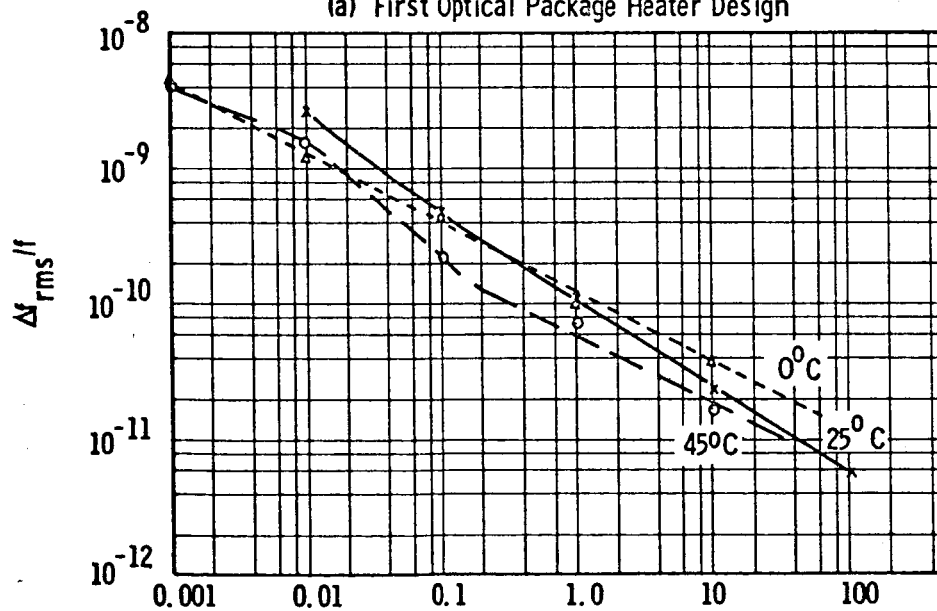
In the course of the program a great deal of experimental data was taken on the breadboard units. In the following sections the results achieved in the final delivered unit are summarized.

2.3.1 Frequency Stability

Short term frequency stability was measured for averaging times ranging from 1 millisecond to 100 seconds and for different environmental temperature conditions. The results of these measurements are shown in Figure 8. Measurements made on the first optical package heater design at ambient temperatures of 25°C and 71°C are shown in Figure 8a. The 25°C measurements show the short term stability varying inversely with the averaging time in the region from 10 to 100 milliseconds and inversely with the square root of the averaging time for times greater than 1 second as is theoretically expected. It is evident from this curve that both the crystal oscillator noise and the noise from the optical package are too large to achieve 5×10^{-12} for a 1 second averaging times. As the temperature is raised the temperature of the photocell in this heater design increases, giving poor signal-to-noise ratio and degrading the short term stability as shown by the 71°C measurements.



(a) First Optical Package Heater Design



(b) Second Optical Package Heater Design

FIGURE 8. SHORT TERM STABILITY MEASUREMENTS

Measurements taken with the second optical package heater design are shown in Figure 8b. In this design, the photocell operates at 80°C as contrasted to photocell temperature of 56 - 75°C with the first heater design. As expected, the short term stability is worse due to the higher photocell operating temperature. The short term stability in this design is very comparable to that obtained at a 71°C ambient temperature in the previous design and the stability is much more constant with fluctuations in the environmental temperature because of the much tighter control of photocell temperature.

Variations of the frequency of the standard with temperature at constant power supply voltage of 28v is shown in Figure 9. With the first optical package design the frequency standard had a frequency change rate of -2×10^{-11} per degree Centigrade at 25°C, with a total frequency deviation over the -34 to +71°C temperature range of approximately 1.6×10^{-9} . With the second optical package design a frequency change rate of -0.6×10^{-11} per degree Centigrade at 25°C was obtained. Total frequency variation with this design is not known outside of the 0 to 45°C region since the unit broke lock due to declining multiplier power before reaching 61°C, and measurements were not made at -34°C due to the tight shipping schedule.

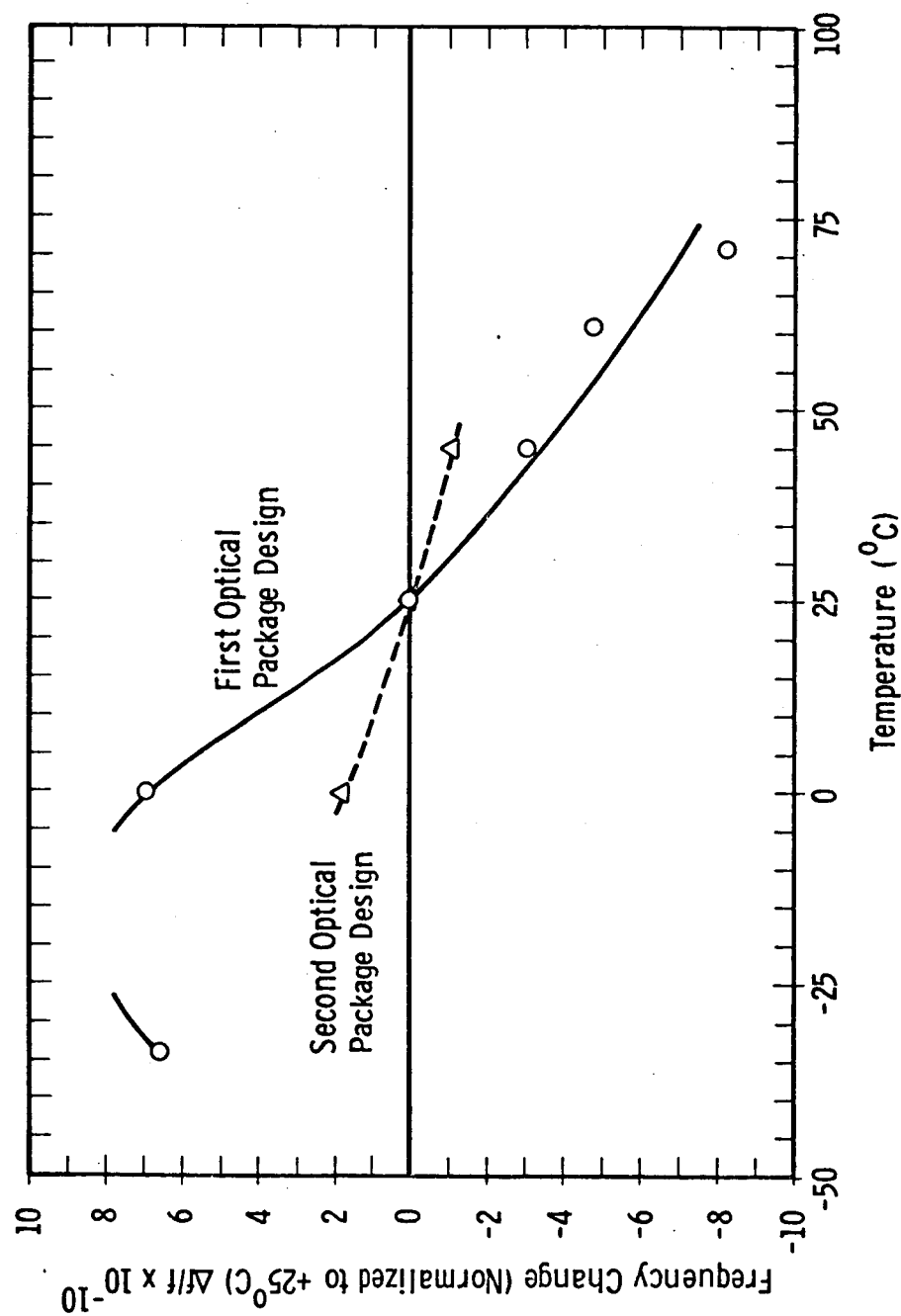


FIGURE 9. FREQUENCY CHANGE VS. TEMPERATURE AT 28V

The variation of the frequency of the standard with power supply voltage at a constant temperature of 25°C is shown in Figure 10. With the first optical package design the frequency varied approximately 2.6×10^{-10} over the 24 to 37 volt range. This was due primarily to variation in the temperature of the filter cell, since the filter cell heater was run directly from the 24 to 37 volt supply. In the second optical package design the variation with voltage was 5.5×10^{-11} , the improvement being due to the fact that the filter cell heater is run from a regulated 6v supply.

Long term stability measurements were not made on the standard. The capabilities of this rubidium system to achieve good long term stability at the high internal operating temperatures is to be established by measurements made at NASA with respect to the hydrogen maser reference over the next one year period.

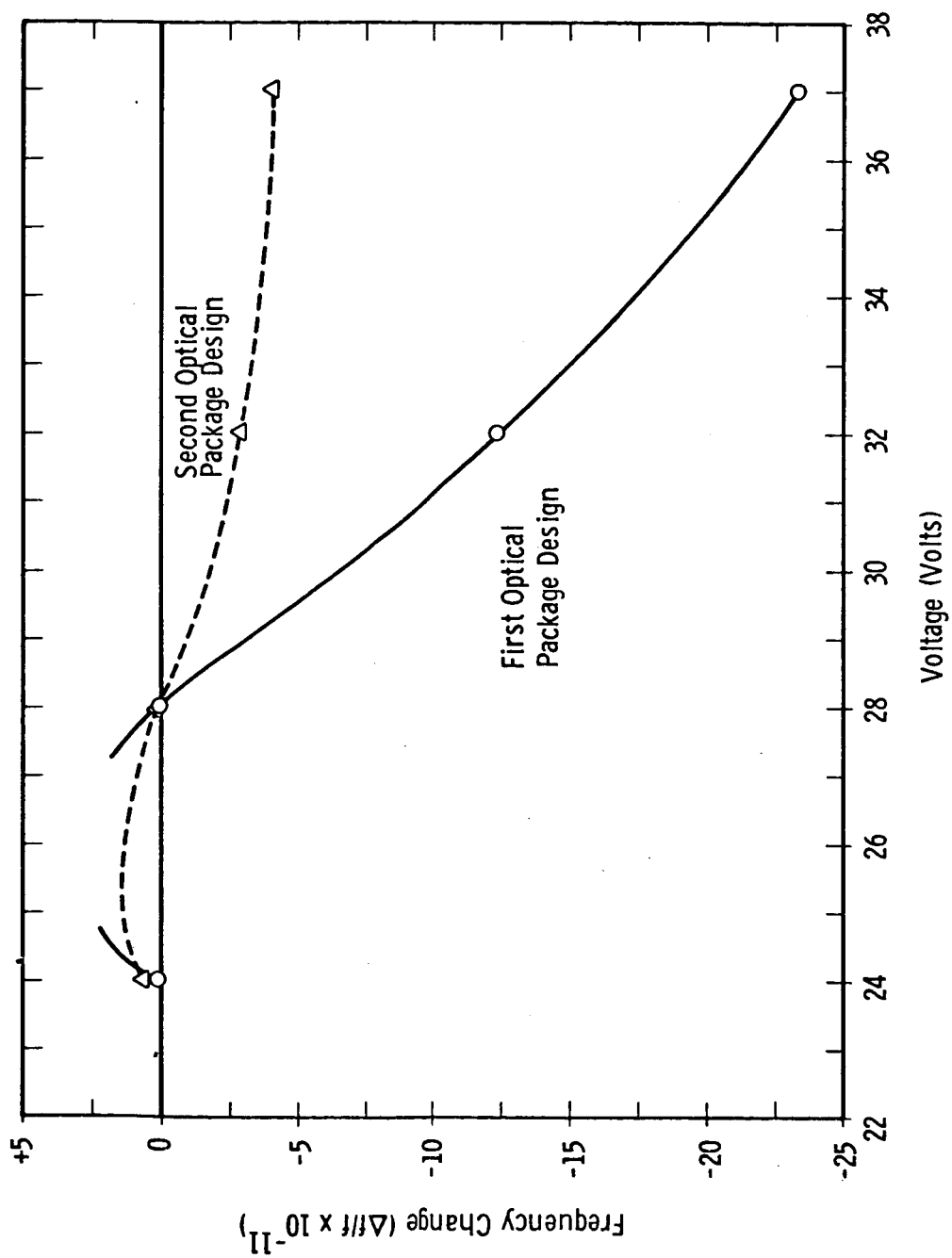


FIGURE 10. FREQUENCY CHANGE VS. VOLTAGE AT 25°C

2.3.2 Power Consumption

The power consumption of the entire space clock as a function of temperature at constant input voltage of 28V which is shown in Figure II. The relatively large variation with temperature is caused by the large amount of power required for the ovens. The variation with temperature was approximately 0.14W per degree centigrade with the first optical package design and 0.20 for the second design. Redesign of the optical package increased power consumption by three watts from 21 to 24 watts at 25°C centigrade. Average input power required for all the circuits excluding the ovens but including the oven controllers is on the order of 9.8W. Power consumption as a function of input voltage for a constant temperature of 25°C is shown in Figure 12. It can be seen that the variation with input voltage particularly with the second optical package is rather small indicating that the efficiency of the power supply and the ovens is quite constant with input voltage.

Power consumption for the various parts of the space clock is summarized in Tables 1 through 3.

2.3.3 Parts Count

The number and category of electronic parts required for the space clock is summarized in Table 4. This table does not include parts in the high frequency multiplier, the crystal oscillator, or the power supply modules, since this information was not obtained from the vendors of these units.

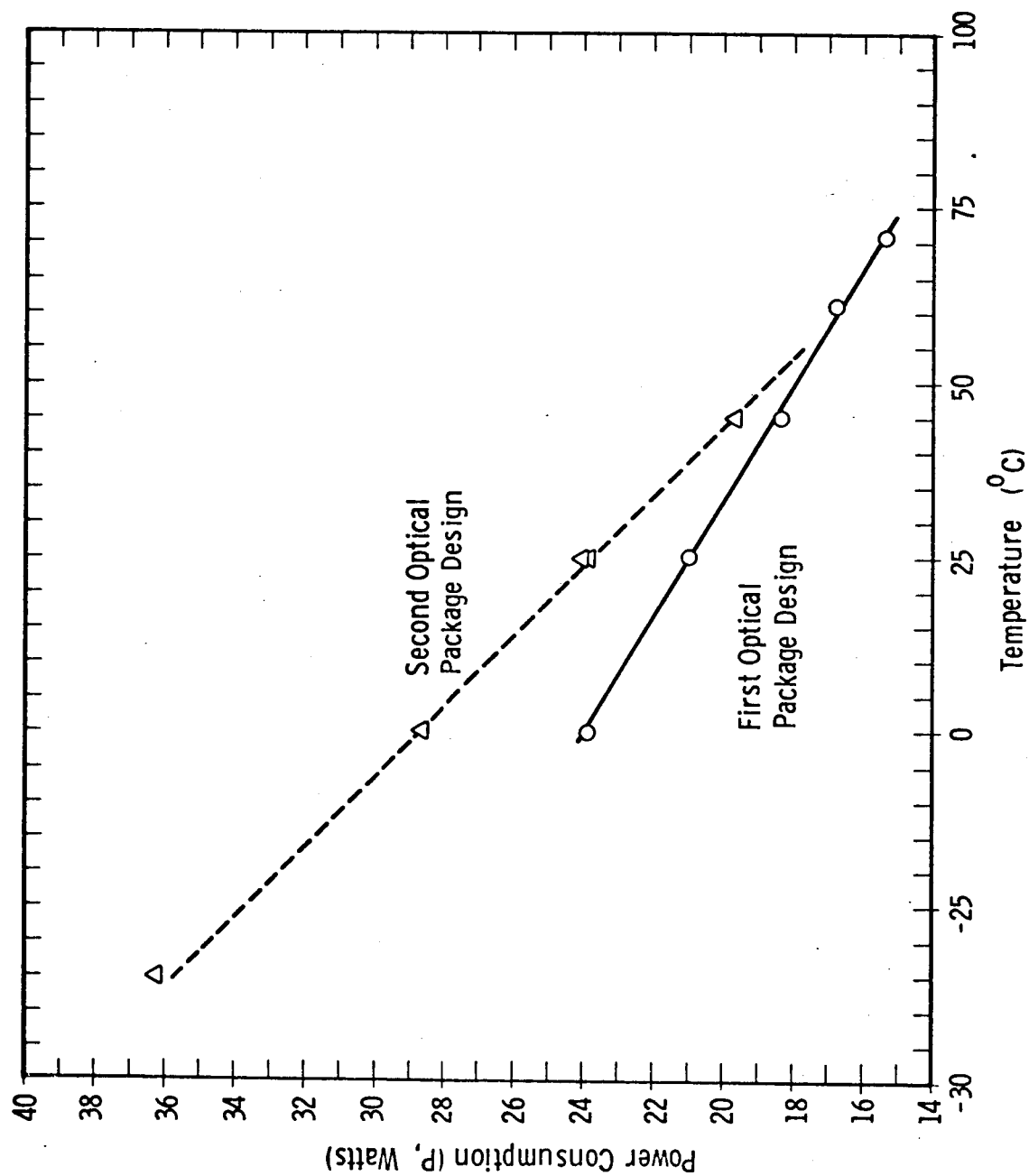


FIGURE 11. POWER CONSUMPTION VS. TEMPERATURE AT 28V

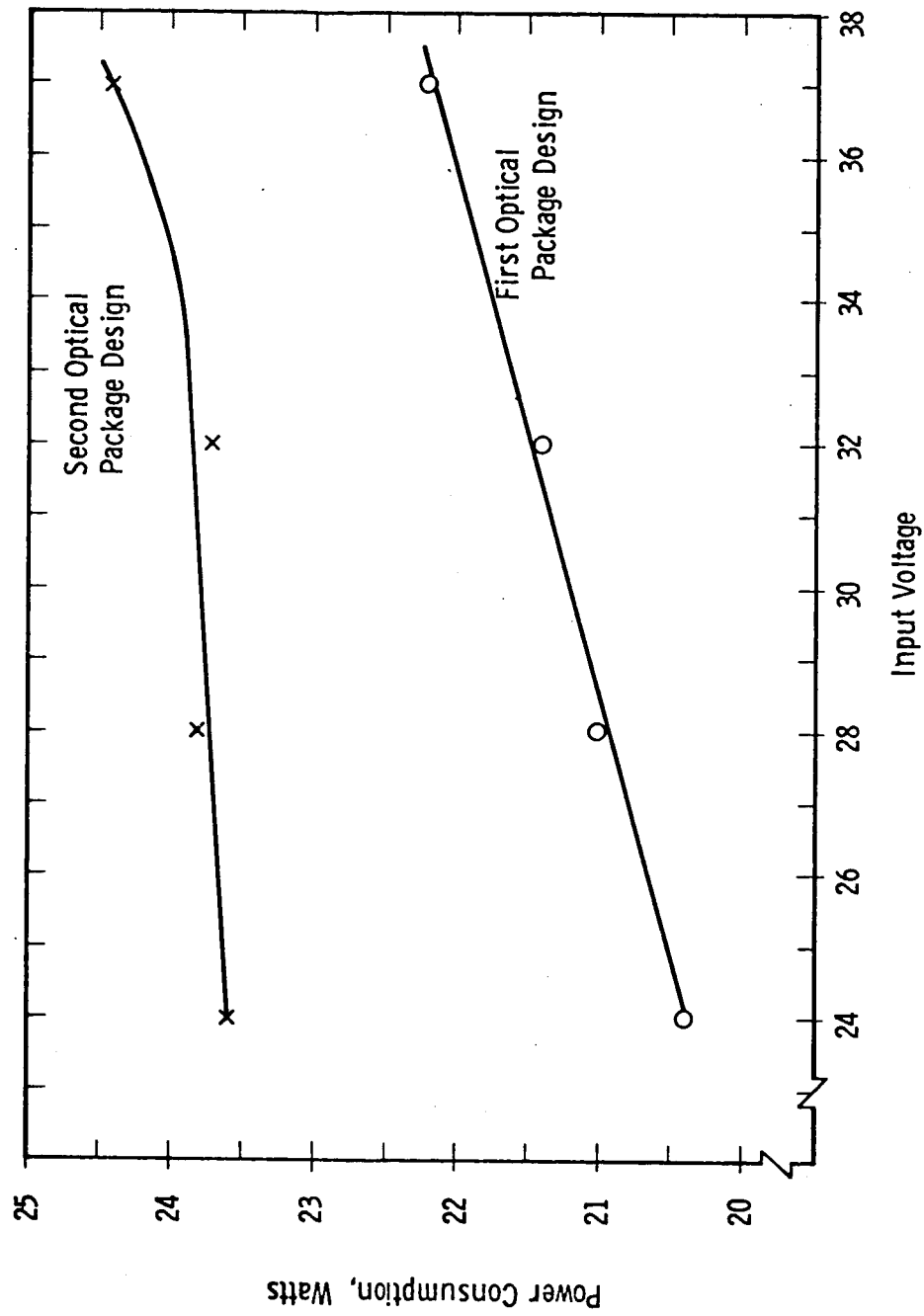


FIGURE 12. POWER CONSUMPTION VS. INPUT VOLTAGE AT 25°C

TABLE I
ELECTRONIC CIRCUITS POWER CONSUMPTION

<u>20V Supply</u>	<u>Current</u>	<u>Power</u>
Servo Amplifier	15mA	0.30W
Crystal Osc. and Temperature Controller	28.5	0.57
Modulation Generator	5	0.10
Multiplier (4.096-20.48MHz)	7.5	0.15
Multiplier (20.48-6834.688MHz)	40	0.80
Synthesizer 14.848MHz	24	0.48
Synthesizer 100KHz	26	0.52
Field Bias	10	0.20
Temperature Controllers:		
Cavity	2.6	0.052
Tip-off	2.6	0.052
Filter Cell	2.6	0.052
Lamp	2.6	0.052
	<hr/> 166.4mA	<hr/> 3.328W
<u>12V Supply</u>		
Lamp Oscillator	60mA	0.72
<u>5V Supply - Low Power</u>		
Divider 16.384-4.096MHz	34mA	0.17W
Divider 4.096-0.512MHz	32	0.16
Output Buffers 4.096-0.512MHz	74	0.37
Lamp Oscillator Bias	2	0.01
	<hr/> 142mA	<hr/> 0.71W

TABLE I - Continued

5V Supply - High Power

Divider and Time Code Generator	60mA	0.300W
Digital part of 100KHz Synthesizer	1.4	0.007
Output Buffers 100KHz - 1Hz	40	0.200
Output Buffers 0.1 sec-200d, IRIGB&E	<u>204</u>	<u>1.020</u>
	305.4mA	1.527W
Total Electronics Power	6.285W	
Total input power for electronics (Regulator 64% efficient)	9.8W	

TABLE 2
OVEN POWER

	-34°C	+25°C	+61°C
Cavity	1.12W	1.06W	1.05W
Tipoff	16.6W	7.5W	2.15W
Filter	0.81W	0.8W	0.79W
Lamp	4.16W	2.9W	2.05W
Oscillator	2.6W	1.6W	0.82W
Total Oven Power	25.29W	13.86W	6.86W

TABLE 3
TOTAL INPUT POWER

	-34°C	+25°C	+61°C
Oven Power	25.3W	13.9W	6.9W
Electronics Input Power	9.8W	9.8W	9.8W
	36.1W	23.7W	16.7W

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COMPONENT BREAKDOWN --- C

	ANALOG CIRCUITS	DIGITAL CIRCUITS	MECHANICAL	OPTICAL CIRCUITS	POWER SUPPLY	TESTING EQUIPMENT	TELETYPE EQUIPMENT	TELETYPE CIRCUITS	TELETYPE CIRCUITS	TELETYPE CIRCUITS	TELETYPE CIRCUITS	TELETYPE CIRCUITS	TELETYPE CIRCUITS
CABLE MOUNT ID	9	2											1
AMP OSCILLATOR	2			1									1
PRE-AMPLIFIER	6	1		1									
Servo AMP.	31	2		20						2			7
Servo AMP.	42	4		21						2			6
14 PH- SWICH	38	2		27	7	2	1			4			7
X 3 MULTIPLIER	11			19	4	5						1	6
100 KHZ SWICH	29	2		20	7	8	4			8			9
TIP AND PUMP	33	4	2	12						8	2		8
SW. & FILE. SW.	35	4	2	10						10	2		8
SIGNAL BOARD				2									
DIGITAL BOARD				1									
DIGITAL BOARD				1									
DIGITAL BOARD				1									
FILE B	6			1									
FILE B				1									
TIME COUNT 17	26			1									18
TIME COUNT 17	26			1									18
FREQUENCY 17	34			7									10
	663	22	4	172	19	21	8	0	40		1		98

TABIE 4-A

TABIE 4 - S A 11 11

	7	6	5	4	3	2	1	Total	Description
								1	
								12	
								80	
			1						
								92	
	1						1	91	
		2						87	
2								77	
2								83	
.		10	3			1		24	
		7	19	1				28	
		12	11	1				24	
		10	2					17	
			30					17	
			1					15	
								55	
								55	
								51	
7	1	14	56	2	1	1		842	total oscillator cylinder & power supply excluded

3. RECOMMENDATIONS FOR DEVELOPMENT WORK IN PART II

The measured results shown in Section 2.3 indicate that the performance of the breadboard is in many respects not as good as that desired in final flight hardware. Consequently, in addition to small packaging of these units, additional development work needs to be carried out in Part II of the contract. In the following sections we defined the design changes which now appear desirable to make.

3.1 DESIGN CHANGES TO BE PERFORMED

Most of the following proposed design changes are intended as improvements to the performance obtained in the breadboard. However, some of the changes are made necessary by changes in the technical specifications requested by NASA.

3.1.1 Optical Package

Additional design work is necessary on the optical package to improve the short term stability, to reduce the temperature sensitivity and to reduce the power consumption. A new mechanical and thermal design of the optical package must be carried out which will utilize the most recent thermal information acquired. This design should use the inner magnetic shield as an outer oven since this was found to significantly improve the temperature sensitivity. It is recommended that the photocell be moved from its present position on the cavity and mounted on the outer oven in order to reduce the temperature and improve the short term stability.

In the present design the light level is well below the level required for optimum broadening. It is believed that this is not due to the low power level at which the lamp runs, since sufficient light was obtained in initial tests using low power lamps in the R-20. The problem appears to be reflection and transmission losses in the rather complicated optical structure which was used to bring the light through the triple magnetic shield. In Part II, studies need to be made of the feasibility of moving the lamp inside the innermost shield and separating the lamp from the lamp oscillator with the latter mounted outside one or more shields. With this design the light pipe can be eliminated, which will increase light level and improve short term stability by a factor of two. Additional improvements may be made by eliminating the microwave wall between the filter and reference cells and by using a different lamp bulb design. If the above change in optical and thermal design are successful, this should lead to a smaller and lighter optical package and less power consumption.

A different philosophy of minimizing the pressure sensitivity of the standard now appears to be feasible. In the present design, the optical package was hermetically sealed to protect it from the environment, the inside was filled with air at atmospheric pressure, and a double walled reference cell was used to protect the cell from pressure variation caused by ambient temperature variations. The problem encountered in this design was that the large amount of glass in the microwave cavity significantly reduced the cavity Q and not enough

multiplier power was available to drive the cavity at its optimum level. It now appears that a better design philosophy would be to use a single walled reference cell in order to obtain higher Q and thus more microwave drive and higher output signal levels, which will improve short term stability. The pressure sensitivity would be minimized by filling the optical package with approximately one-tenth of an atmosphere of dry nitrogen and sealing this unit. No significant pressure change due to out-gassing will be encountered with this large an internal pressure, yet internal pressure is low enough to prevent temperature variations from causing significant frequency changes.

3.1.2 Power Supply Redesign

A change in the power supply philosophy is necessary to accommodate a number of changes in electrical specifications requested by NASA between part I and part II. These changes are:

- 1) D.C. isolation between the input power and the output signals
- 2) Operation down to 22V instead of 24V
- 3) A restriction on the maximum current feedback ripple in the power supply lines
- 4) Specification that the unit shall operate within specifications rather than survive input voltage transients on the power supply line.
- 5) Addition of an input voltage ripple specification of 4V p-p square wave.
- 6) Addition of short circuit protection on all of the output signal lines.

In the present power supply design shown in Figure 2, heater power is drawn directly from the input power lines. This requires that the heaters have a common ground with the 20V regulated supply from which the heater controllers operate. This supply must in turn have a common ground with the 5V supplies from which the output amplifiers operate because of the AC signal coupling between the crystal oscillator, which runs on 20V, and the divider chain, which runs on 5V.

In addition, the case must be connected to the negative side of the 20 and 5V supplies since it forms shielding for some of the high frequency circuits. Thus, no D.C. isolation exists between the input power, the regulated D.C. lines, the output signals, or the case. This design approach was chosen in order to minimize power consumption, since the heater power is drawn directly from the input line and does not have to undergo the inefficiency of a converter.

A block diagram of the proposed power supply configuration is shown in Figure 13. In this design, D.C. input power is pre-regulated by a ripple regulator which also provides reverse polarity protection. The output of the pre-regulator at approximately 18V D.C. drives a D.C. to D.C. converter oscillator. All power for the clock is coupled through the oscillator transformer which provides D.C. isolation between the input power lines and all other parts of the clock. Dissipative regulators supply output D.C. voltages of 20, 12, 6 and 5V. The 6V supply replaces one of the present 5V supplies in order to enable short

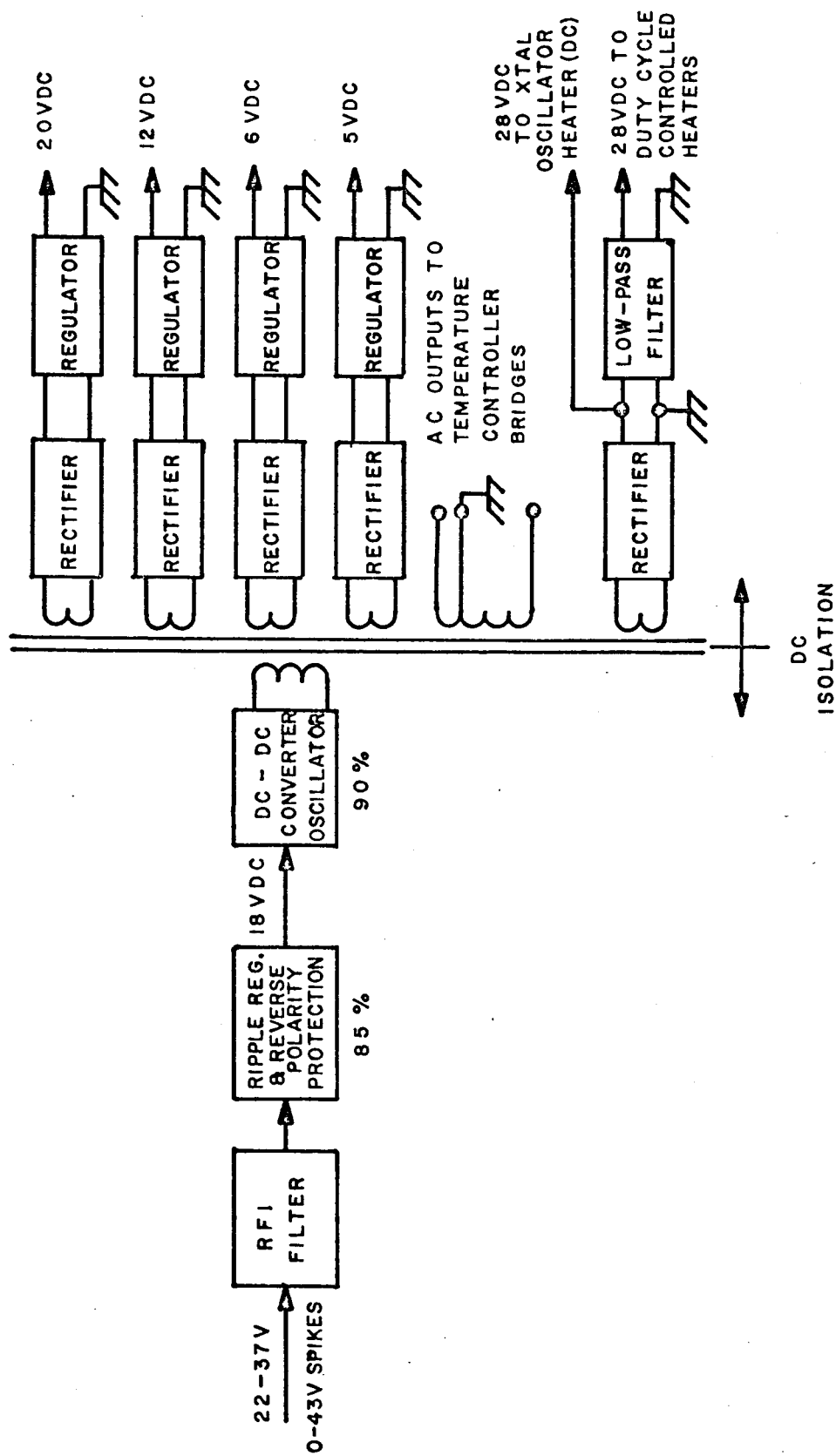


FIGURE 13—BLOCK DIAGRAM- PROPOSED POWER SUPPLY CONFIGURATION

circuit protection to be established for all of the 5V p-p digital output lines. A.C. outputs to the temperature controller bridges will be supplied as in the present power supply. The present low power 6V supply which is used for the filter cell heater is replaced by a 28V supply which provides power for all of the heaters in the clock. This design requires that the D.C. to D.C. converter be a substantially higher power unit than in the present design, and it also means that the heater power encounters the inefficiencies of the ripple regulator, the D.C. to D.C. converter, and the rectifier filter combination, for an overall efficiency of approximately 72%. This increases the total input power substantially. A low pass filter is used in series with the duty cycle heaters in order to prevent the large current pulses from affecting the crystal oscillator heater, which is taken off ahead of the low pass filter, and also from affecting the other outputs taken from the D.C. to D.C. converter transformer. This design eliminates the large current pulses taken from the input power supply line and enables the input current ripple specification to be met. It also solves the problem of input voltage transients and square wave input voltage ripple from affecting the power supply outputs. All outputs from the D.C. to D.C. converter have common ground connections which are identical to the case ground. Because of this common ground arrangement, it may be desirable to use a single Zener reference for all regulators and for the field bias control circuit in order to minimize power consumption. This Zener could be mounted in the crystal oscillator in order to obtain better

temperature control and therefore better voltage stability over the environmental temperature range.

3.1.3 Other Circuit Redesign

A different crystal oscillator should be evaluated in Part II. It is believed that the short term stability of the oscillator can be significantly improved and the size and power consumption may be somewhat reduced. In addition, the Zener reference may be incorporated inside as indicated above. It may also be possible to use a single output amplifier to drive both the divider and the synthesizer and thus obtain a more efficient circuit.

More work needs to be done on the multiplier to minimize its power variation with temperature. With the present design adequate performance appears possible based on measurements taken on similar units, however, this performance has not been achieved in the units used in the breadboard clocks.

Layout and plug connection philosophy needs to be evaluated in order to minimize the frequency steps that are caused by disconnecting the monitor and control cable from the test and calibration unit.

The possibility of eliminating the controller for the cavity heater and supplying this heater with a fixed amount of power will be investigated. This would simplify the circuitry and slightly improve the power consumption.

The digital circuits require a small amount of re-design to enable the clock to reset at 365 or 366 day intervals as requested by NASA. In addition, the low frequency digital circuits and their output amplifier will be run from the 6V supply in order to obtain short circuit protection on these outputs. Careful grouping of the digital circuits is to be carried out to obtain optimum packaging density and minimization of cross talk between lines. Dual flip-flops are to be used in place of the present single flip-flops, and this will significantly improve the parts count and packaging density.

3.1.4 Mechanical Design and Packaging

A major portion of the work in Part II is that of packaging the space clock. It is anticipated that Cannon Chico-pac modules can be used for high density packaging of the digital circuits, and this construction may be extended to the analog circuits. The overall package is to be hermetically sealed to protect it from the various environment conditions and is to incorporate rfi barriers. The latter presents a problem because of the large number of output lines, all of which would require rfi filtering if the rfi barrier encompasses the whole clock. These filters significantly contribute to the size and weight of the unit. At present it is proposed to have the entire frequency standard portion inside the rfi barrier and include the divider chain and output amplifiers down to the 1Kc point. The lower frequency circuits and output amplifiers would therefore be outside the rfi barrier.

3.2 Recommended Revision of Specifications

The work on part I of the contract has indicated that there are some areas in which the present specifications will not adequately describe the performance of the unit, and other areas in which the combination of desired difficult specifications cannot be simultaneously achieved. Recommendations for revisions in the specifications which take into account the present state of the art as determined by the work performed on part I of the contract, are presented below. In addition, recommendations for maximum contractual specifications in areas which were previously defined only by design goals are made.

3.2.1 Long Term Stability

The present long term stability specification is written in such a manner that it includes frequency changes due to ambient temperature cycling. Since variations of frequency over the total environmental temperature range are expected to be the same order of magnitude as the frequency change at constant temperature over a period of one year, the intertwining of these two specifications does not give a reasonable specification on either one. Separate specifications will provide a better understanding of the performance characteristics of the standard for systems analysis, and will be in accordance with current practice in specifying commercial atomic and crystal standards. We recommend that the long term stability specification remain as written in the contract as 5×10^{11} rms variation in the daily average frequencies taken over a period of one year. We propose a new speci-

fication defining the maximum change in frequency over the environmental temperature range of 1×10^{10} maximum. This latter specification has not been achieved in the breadboard unit but appears to be a reasonable maximum limit following further development work.

3.2.2 Short Term Stability

As expressed in sections 2.2 and 2.3 above, major problems were encountered in attempting to operate the optical package at high internal temperatures without degrading the short term stability. The present contract specification calls for an improved short term stability of approximately a factor of 2 over the existing state-of-the-art in present commercial rubidium standards. It has become clear that an improvement in short term stability in combination with higher ambient operating temperatures is beyond the present state-of-the-art, and it is proposed that the short term stability specification be revised to 3×10^{11} rms for one second averaging times. Again, this level is not achieved in the breadboard unit, but appears to be a reasonable maximum limit based on several areas in which improvements can be made in part II of the contract.

3.2.3 Size, Weight and Power Consumption

Specifications on size, weight and power consumption as they presently exist are all target specifications. For system design it is important to have maximum limits in all three of these areas. The work on the breadboard unit has shown that the optical package will

be the largest contributor to all three of these specifications. It is also clear that in designing the optical package for the difficult combination of characteristics, particularly minimum power consumption, tight internal temperature control, and insensitivity to shock and vibration, the unit must be larger, heavier, and consume more power than had originally been thought possible. Consequently we propose as maximum specifications for the space clock, a weight of 25 lbs., a volume of 600 cubic inches, and a power consumption of 30 watts above 75°F and 42 watts from -30°F to +75°F. These specifications are maximum limits only, and typical performance will be better than these limits.

4.0 CONCLUSION

A great deal has been accomplished in part I of the program in determining and advancing the state-of-the-art in rubidium frequency standards designed for the combination of high temperature operation, wide temperature range, miniaturization, and rugged mechanical design. The proposed technical specifications plus the revisions proposed by NASA in certain design concepts to make the unit more suitable for incorporation into future spacecraft systems should result in an atomic time and frequency system which is well suited for future space missions. Part II of the contract is to be carried out by General Radio, under supervision of Varian personnel, and we are confident in their competence to meet the specifications and build units for use onboard spacecraft which will be satisfactory to NASA in every way.